AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. **(canceled)**

2. (previously presented) The flip chip package as claimed in claim 4, wherein the semiconductor chip is mechanically and electrically interconnected to the chip contact pads of the substrate via solder joints.

3. (original) The flip chip package as claimed in claim 2, further comprising an underfill formed between the semiconductor chip and substrate.

4. **(currently amended)** A flip chip package, comprising:

a substrate having an upper surface and a lower surface, the substrate comprising:

a recessed cavity defined in the upper surface of the substrate;

a reinforcement-containing insulating layer;

a plurality of chip contact pads formed on the surface of the reinforcement-containing insulating layer and exposed from the recessed cavity; and

a plurality of solder pads formed on the upper surface of the substrate and outside the recessed cavity for making external electrical connections;

wherein the chip contact pads are electrically connected to the solder pads; and

a semiconductor chip disposed in the recessed cavity of the substrate by flip chip bonding

and electrically connected to the chip contact pads;

said package further comprising a metal coating formed on the lower surface of the substrate and a plurality of conductive vias formed through the reinforcement-containing insulating layer and electrically connecting the metal coating and the chip contact pads.

5. (previously presented) The flip chip package as claimed in claim 4, further comprising a heat sink disposed on top of the semiconductor chip.

6. (previously presented) The flip chip package as claimed in claim 4, wherein the reinforcement-containing insulating layer is formed from BT (bismaleimide-triazine) resin.

7. (previously presented) The flip chip package as claimed in claim 4, wherein the reinforcement-containing insulating layer is formed from FR-4 fiberglass reinforced epoxy resin.

8. (previously presented) The flip chip package as claimed in claim 4, wherein the conductive vias extend through an entire thickness of the insulating layer.

9. (previously presented) The flip chip package as claimed in claim 4, further comprising conductive traces being formed on the upper surface of the insulating layer and electrically connecting the chip contact pads to the solder pads;

wherein the conductive vias extend from the metal coating, through the insulating layer, to said conductive traces.

10. (previously presented) The flip chip package as claimed in claim 9, wherein said substrate further comprises conductive circuit patterns formed outside said cavity and, together with said conductive traces, electrically connecting the chip contact pads to the solder pads.

11. **(currently amended)** A flip chip package, comprising:

a substrate comprising

a first layer including internal conductive circuit patterns;

a second layer which is an insulating layer positioned below the first layer;

a cavity formed in the first layer;

a plurality of chip contact pads formed in the cavity and on an upper surface of the insulating layer;

a plurality of solder pads formed on an upper surface of the first layer and outside the cavity for making external electrical connections;

a metal coating formed on a lower surface of the insulating layer; and

a plurality of conductive vias extending through an entire thickness of the insulating layer and electrically connecting the metal coating and the chip contact pads;

wherein the chip contact pads are electrically connected to the solder pads via the internal conductive circuit patterns of the first layer; and

a semiconductor chip disposed in the cavity and electrically connected to the chip contact pads.

12. (previously presented) The flip chip package as claimed in claim 11, wherein the semiconductor chip is mechanically and electrically connected to the chip contact pads via solder joints.

13. (previously presented) The flip chip package as claimed in claim 12, further comprising an underfill formed between the semiconductor chip and the insulating layer.

14. (previously presented) The flip chip package as claimed in claim 11, further comprising conductive traces being formed on the upper surface of the insulating layer and,

together with said internal conductive circuit patterns, electrically connecting the chip contact pads to the solder pads;

wherein the conductive vias extend from the metal coating, through the insulating layer, to said conductive traces.

15. (previously presented) The flip chip package as claimed in claim 11, further comprising a heat sink disposed on top of the semiconductor chip.

16. (previously presented) The flip chip package as claimed in claim 11, wherein the insulating layer is formed from BT (bismaleimide-triazine) resin.

17. (previously presented) The flip chip package as claimed in claim 11, wherein the insulating layer is formed from FR-4 fiberglass reinforced epoxy resin.

18. (previously presented) The flip chip package as claimed in claim 11, wherein said metal coating defines an outer most surface of said package.

19. (previously presented) The flip chip package as claimed in claim 15, wherein said conductive vias define, in addition to said heat sink, another heat conducting path through which heat generated by the chip in operation can be conducted to the metal coating to be dissipated to an outside of said package.

20. (previously presented) The flip chip package as claimed in claim 11, wherein said metal coating defines an outer most surface of said package.

21. (previously presented) The flip chip package as claimed in claim 5, wherein said conductive vias define, in addition to said heat sink, another heat conducting path through which heat generated by the chip in operation can be conducted to the metal coating to be dissipated to an

outside of said package.